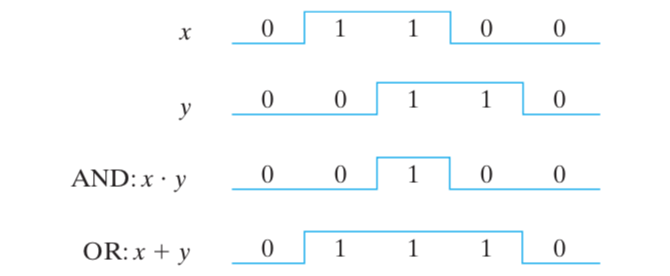
Name (Pin Yin): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student ID \_\_\_\_\_\_\_ Grade: \_\_\_\_\_\_

**CQUPT EE310 2020 Fall Quiz 1a**

**(15min, 20pts)**

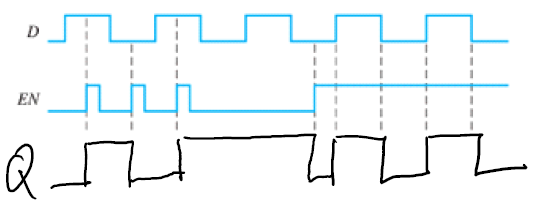
1. ((4pts) Inputs x & y are shown by the waveforms below. Draw the waveform for the output function (x OR y)



1. (4pts) Apply DeMorgan’s law to the expression: 2pts each step
2. (4pts) Write the truth table of a 4-to-1 multiplexer. -1pt each error

|  |  |  |  |
| --- | --- | --- | --- |
| EN | S1 | S0 | Y |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

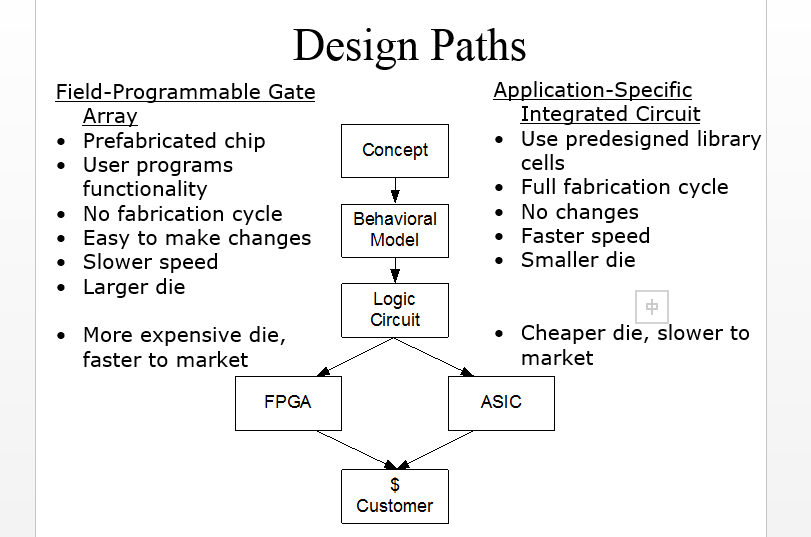
1. (4pts) Draw the output waveform Q for the given gated SR latch below. Q is 0 initially! -2pts if minor error, -4 if answer makes no sense



1. (4pts) What is the main difference between FPGA and ASIC? Check graph next page, if the difference is mentioned but not the key different, -1pt

FPGA: hardware is ready before the design

ASIC: Need to go through the whole fabrication process

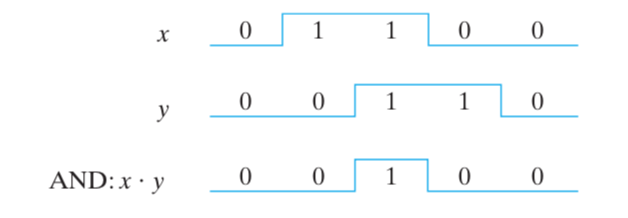


Name (Pin Yin): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Assign. No. \_\_\_\_\_\_\_ Grade: \_\_\_\_\_\_

**CQUPT EE310 2020 Fall Quiz 1b**

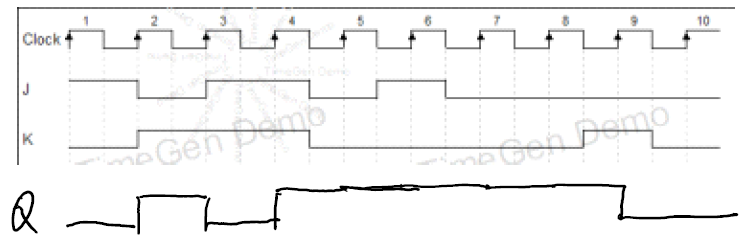
**(15min, 20pts)**

1. (4pts) Inputs x & y are shown by the waveforms below. Draw the waveform for the output function (x AND y)



1. (4pts) Apply DeMorgan’s law to the expression: -2pts if not get the final result
2. (4pts) Write the truth table of a 2-to-4 decoder. -1pt each error

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| EN | I1 | I0 | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

1. (4pts) Draw the output waveform Q for the given JK flip-flop below. Q is 0 initially! -2pts if minor error, -4 if answer makes no sense 
2. (4pts) What is the main difference between FPGA and ASIC? Check graph next page, if the difference is mentioned but not the key different, -1pt

FPGA: hardware is ready before the design

ASIC: Need to go through the whole fabrication process

